LISTING OF CLAIMS

1. (Canceled)

2. (Currently amended) The method according to claim [[1]] 5, further comprising etching the underlying layer using the mask line to define formation of the integrated circuit line from the underlying layer.

3. (Original) The method according to claim 2, wherein the integrated circuit line has a critical dimension of less than 0.25 microns.

4. (Original) The method according to claim 2, wherein the integrated circuit line has a critical dimension of about 0.06 microns or less.

5. (Currently amended) A method of forming an integrated circuit line on a wafer using a lithographic technique, comprising:

providing the wafer, the wafer including a substrate and, over the substrate, each of a photo resist layer and an underlying layer to be processed under the photo resist layer;

exposing and developing the photo resist layer to form a photo resist line, the photo resist line having a line width smaller than a desired line width of the integrated circuit line;

coating the photo resist line with a reactive coating; and

reacting the photo resist line with the coating to form a mask line having a line width corresponding to the desired line width of the integrated circuit line and with a smaller line edge roughness (LER) than of the photo resist line; and ~~The method according to claim 1,~~

wherein a difference between a critical dimension of the photo resist line and a critical dimension of the mask line is about 30 nanometers to about 60 nanometers.

6. (Currently amended) A method of forming an integrated circuit line on a wafer using a lithographic technique, comprising:

providing the wafer, the wafer including a substrate and, over the substrate, each of a photo resist layer and an underlying layer to be processed under the photo resist layer;

exposing and developing the photo resist layer to form a photo resist line, the photo resist line having a line width smaller than a desired line width of the integrated circuit line;

coating the photo resist line with a reactive coating;

reacting the photo resist line with the coating to form a mask line having a line width corresponding to the desired line width of the integrated circuit line and with a smaller line edge roughness (LER) than of the photo resist line; and ~~The method according to claim 1, further comprising~~

optimizing a change in critical dimension from the photo resist line to the mask line with an amount of LER improvement from the photo resist line to the mask line.

7. (Original) The method according to claim 6, wherein the optimizing includes at least one of selecting a material for the photo resist layer, controlling an exposure pattern to achieve a desired critical dimension of the photo resist line, and controlling an amount of reaction between the photo resist line and the coating.

8. (Original) The method according to claim 6, wherein the optimizing includes controlling an amount of reaction between the photo resist line and the coating.

9. (Original) The method according to claim 8, wherein the controlling includes at least one of controlling a coating thickness, controlling a post application bake time and temperature, controlling a mixing bake time and temperature, and controlling a post development bake time and temperature.

10. (Currently amended) A method of forming an integrated circuit line on a wafer using a lithographic technique, comprising:

providing the wafer, the wafer including a substrate and, over the substrate, each of a photo resist layer and an underlying layer to be processed under the photo resist layer;

exposing and developing the photo resist layer to form a photo resist line, the photo resist line having a line width smaller than a desired line width of the integrated circuit line;

coating the photo resist line with a reactive coating;

reacting the photo resist line with the coating to form a mask line having a line width corresponding to the desired line width of the integrated circuit line and with a smaller line edge roughness (LER) than of the photo resist line; and ~~The method according to claim 1, further comprising~~

accounting for changes in an end of the photo resist line caused by reaction with the coating using optical proximity correction.

11. (Currently amended) The method according to claim [[1]] 5, wherein the coating is a shrink coating.

12. (Currently amended) The method according to claim [[1]] 5, wherein the reacting includes exposing the wafer to a temperature of about 105 degrees C to about 120 degrees C for about sixty seconds to about seventy seconds.

13. (Currently amended) The method according to claim [[1]] 5, wherein the reacting includes exposing the wafer to a temperature of about 112 degrees C to about 120 degrees C.

14. (Currently amended) The method according to claim [[1]] 5, further comprising, after reacting, rinsing the wafer with one of deionized water, deionized water and a surfactant, deionized water and isopropyl alcohol, and mixtures thereof.

15. (Currently amended) The method according to claim [[1]] 5, wherein the integrated circuit line is a conductive line used to form at least one gate electrode or an addressable word line.